IN THE CLAIMS

1-4. (canceled)

5. (currently amended) An apparatus comprising:

plural buffers;

a Central Processing Unit (CPU) for causing packets arriving from a network at said apparatus to each be stored in a separate one of the buffers, the CPU also being arranged to calculate~~, upon receipt of every Nth packet of data,~~ an optimal delay to guarantee a predetermined probability of packet loss and provide a minimum buffer latency, beyond which a packet will be discarded, the optimal delay being calculated ~~using~~ based at least in part on a probability distribution that is updated upon the receipt of each packet ; and

a timer for causing each packet to incur an added delay of at least the difference between the ~~calculated~~ optimal delay and an actual network delay experienced by said each packet.

6. (canceled)

7. (canceled)

8. (previously presented) The apparatus of claim 5 further comprising a network interface card coupled to the CPU for receiving signals from the data network.

9. (previously presented) The apparatus of claim 5 wherein the CPU is a Digital Signal Processing (DSP) chip that performs DSP, CPU control and input/output functions.

10. (previously presented) The apparatus of claim 8 wherein said network interface card implements the G.723 or G.729 standard.

11. (currently amended) A method of processing packets comprising:

receiving [[a]] packets from a network;

ascertaining a network delay incurred by each packet in traversing the network;

updating a probability distribution of packet delays through the network;

~~updating~~ adapting an optimal delay to guarantee a predetermined probability of packet loss and provide a minimum buffer latency for each packet, wherein the minimum buffer latency ~~that~~ is based at least in part on the updated probability distribution;

~~reading information in the packet and ascertaining therefrom a delay incurred by the packet in traversing the network~~;

~~comparing the delay ascertained to the optimal delay;~~

placing the packet into a buffer; and

delaying use of the packet ~~to reconstruct a signal by a calculated~~ by an amount of time ~~sufficient to make the calculated amount plus the ascertained delay~~ substantially equal to the optimal delay minus the network delay.

12. (canceled)

13. (currently amended) The method of claim 11 wherein ~~said required~~ the minimum buffer latency ~~delay~~ is recalculated every Nth packet.

14. (currently amended) The method of claim 13 further comprising comparing ~~said~~ the minimum ~~delay~~ buffer latency to a predetermined value each time ~~said~~ the minimum ~~delay~~ buffer latency is recalculated, and, if ~~said~~ the recalculated minimum ~~delay~~ buffer latency exceeds said predetermined value, assigning ~~said required minimum delay~~ the minimum buffer latency to be said predetermined value.

15. (currently amended) A gateway comprising:

a buffer for storing ~~said~~ received packets;

a CPU for updating a probability distribution of packet delays through a network upon the receipt of each packet and for calculating a delay to which each of a plurality of received packets should be subjected before being read out of the buffer;

a timer for subjecting each packet to [[a]] the calculated delay ~~that equals~~ which is equal to an optimal delay, the optimal delay being dynamically updated to guarantee a predetermined probability of packet loss and provide a minimum buffer latency based at least in part on the updated probability distribution, minus a network delay experienced by the packet, unless such calculated delay exceeds a predetermined maximum, in which case the predetermined maximum is utilized as the calculated delay.

16. (previously presented) A method of measuring varying delays among a plurality of packets, comprising:

receiving a first packet at a receiving gateway;

maintaining constant any synchronization error between a transmitting gateway and the receiving gateway by inserting a delay said packet is estimated to have experienced in traversing a network; and

setting a clock at said receiving gateway to a value equal to a time stamp contained within said first packet plus said estimated delay.

17. (previously presented) The method of claim 16 further comprising receiving packets in addition to said first packet, reading a time stamp from each of said additional packets, calculating a network delay for each of said additional packets based upon said clock at said receiving gateway and said timestamp from each of said additional packets.

18. (previously presented) The method of claim 16 further comprising updating a probability distribution function indicative of network delays after receipt of every Nth packet.

19. (canceled)

20. (original) The method of claim 18 wherein said updating further comprises recalculating a buffer latency.

21. (previously presented) The method of claim 20 wherein said buffer latency is assigned a value different from the recalculated buffer latency only if said recalculated buffer latency exceeds a predetermined value.

22. (currently amended) An apparatus comprising:

a signal processor for calculating a delay experienced by each of a plurality of packets through a data network; and

a buffer system for delaying further conveyance of each of said packets according to a minimum buffer latency which is time dependant on the calculated delay and an optimal delay, the optimal delay being adapted according to ~~by an amount of time dependant upon (1)~~ a probability distribution updated in response to receipt and processing of selected ones of each of said packets~~, and (2) said calculated delay~~.

23. (original) Apparatus of claim 22 wherein said buffer system is arranged to delay further conveyance by an amount also dependant upon a prestored maximum.

24. (canceled)

25. (original) Apparatus of claim 23 further comprising an interrupt generator for generating an interrupt when said amount of time for said each packet expires.

26. (original) Apparatus of claim 23 further comprising a poller for sequentially polling each of a plurality of storage locations within said buffer system to determine if a packet within said storage location is to be further conveyed.

27. (withdrawn) Timing apparatus comprising:

a processor for reading a time stamp in a received data packet, and for setting a clock a specified amount ahead of said time stamp; and

a receiver for receiving subsequent data packets and measuring delay by comparing a time stamp in each of said subsequent packets to said clock.

28. (withdrawn) Timing apparatus of claim 25 wherein said specified amount is programmed to be a delay indicative of a delay experienced by a packet through a data network.

29. (withdrawn) Timing apparatus of claim 27 further comprising a signal processor for converting data within said received packet and within said subsequent packets to an audio signal.